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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,580	08/05/2003	Motoko Tanishima	108066-00096	5431

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ARENT FOX PLLC
1050 CONNECTICUT AVENUE, N.W.
SUITE 400
WASHINGTON, DC 20036

EXAMINER	
PHAM, LY D	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 05/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,580	TANISHIMA ET AL.	
	Examiner	Art Unit	
	Ly D. Pham	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) *6-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8-5-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's Information Disclosure Statement, IDS, filed August 05, 2003 has been considered by the Examiner.

Election/Restrictions

2. Claims 6 – 11 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Claims 1 – 5 have been elected **without** traverse in the reply filed on March 18, 2005.

3. Claims 1 – 5 are presented for the Examination.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 – 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Choi et al. (US Pat 5,297,085).

Regarding **claim 1**, Choi et al. disclose a memory circuit comprising:

a regular memory cell array (col. 1, lines 49 – 52, 'a plurality of normal blocks containing only normal memory cells...');

a redundant memory cell array which enables to replace a failed portion in the regular memory cell array (col. 1, lines 52 – 53);

a redundant replacement memory for storing data on the failed portion in the regular memory cell array (col. 2, lines 6 – 15, '... redundant column decoder being programmed to select redundant columns replacing normal columns which are containing defective normal memory cells according ...'. The redundant column decoder in itself also acts as a redundant replacement memory!)

a pre-charge circuit disposed in the regular memory cell array (col. 2, lines 27 – 29, 'normal precharge circuits connected to the normal column lines in the respective normal block'),

wherein depending on the data on the failed portion, the failed portion in the regular memory cell array is replaced with the redundant memory cell array (col. 1, lines 54 – 59), while a pre-charge path is closed which leads to the pre-charge circuit corresponding to the failed portion (col. 2, lines 25 – 39, 'redundant precharge circuit... when a defective normal cell is addressed, all of the normal precharge circuits are disabled...').

Regarding **claim 2**, Choi et al. also disclose the memory circuit according to claim 1, wherein:

the regular memory cell array has a plurality of redundant replacement units and is replaced with the redundant memory cell array for each redundant replacement unit

having the failed portion (col. 1, lines 54 – 59, 'the plurality of normal blocks—units, each to be replaced with the redundant block—redundant memory cell array),

the redundant replacement memory outputs a redundant replacement specify signal for specifying the redundant replacement unit having the failed portion (col. 2, lines 6 – 25, '...output signals of the block decoder and second address signals'), and

the pre-charge circuit has a pre-charge switch for each redundant replacement unit so that the pre-charge switch corresponding to the redundant replacement unit having the failed portion is turned off by the redundant replacement specify signal (col. 2, lines 25 – 39, 'When a defective normal cell is addressed, all of the normal precharge circuits are disabled in response to the redundant control clock').

Regarding **claim 3**, Choi et al. also disclose the memory circuit according to claim 2, wherein when the redundant replacement unit having the failed portion is replaced with the redundant memory cell array, a pre-charge switch corresponding to the redundant memory cell array conducts (col. 2, lines 25 – 39, redundant precharge circuit in operation when a defective normal cell is addressed).

Regarding **claim 4**, Choi et al. also disclose the memory circuit according to claim 1, wherein the regular memory cell array and the redundant memory cell array having a plurality of memory cells and a plurality of bit lines connected to the plurality of memory cells, the plurality of bit lines being pre-charged by the pre-charge circuit (col. 1, line 67 – col. 2, line 6, and col. 2, lines 25 – 30).

Regarding **claim 5**, Choi et al. also disclose the memory circuit according to claim 4, wherein the memory cell is a static memory cell (col. 3, lines 12 – 19, SRAM—Static RAM).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See also Hidaka (US Pat 6,469,923 B1) col. 1, lines 27 – 32 for the claimed feature of redundant replacement memory for storing data on the failed portion in the regular memory cell array.

7. When responding to the office action, Applicant(s) are advised to provide the examiner with the page and line numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

8. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D. Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly Pham
May 16, 2005

HOAI HO
PRIMARY EXAMINER